EXHIBIT A: CLEAN VERSION OF SUBSTITUTE SPECIFICATION

SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS

INVENTORS

Tae Heon Lee
Mu Hwan Seo

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a divisional of U.S. Application Serial No. 09/687,585 entitled SEMICONDUCTOR PACKAGE HAVING REDUCED THICKNESS filed October 13, 2000.

STATEMENT RE: FEDERALLY SPONSORED RESEARCH/DEVELOPMENT

[0002] Not Applicable

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

[0003] The present invention relates to a semiconductor package and, more particularly, but not by way of limitation, to a semiconductor package that has a reduced thickness.

2. HISTORY OF RELATED ART

[0004] It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package. A primary